LINEAR TECHNOLOGY

DESIGN NOTES

Accurate Power Supply Sequencing Prevents System Damage

Design Note 384

Jeff Heath and Akin Kestelli

Introduction

Many complex systems—such as telecom equipment, memory modules, optical systems, networking equipment, servers and base stations—use FPGAs and other digital ICs that require multiple voltage rails that must start up and shut down in a specific order, otherwise the ICs can be damaged. The LTC®2924 is a simple and compact solution to power supply sequencing in a 16-pin SSOP package (see Figures 1 and 2).

How it Works

Four power supplies can be easily sequenced using a single LTC2924 and multiple LTC2924s can be just as easily cascaded to sequence any number of power supplies. With slightly reduced functionality, six power supplies can be sequenced with a single LTC2924.

The LTC2924 controls the start-up and shutdown sequence and ramp rates of four power supply channels via output pins (OUT1 to OUT4). Each OUT pin uses a 10µA current source connected to an internal charge pump and a low resistance switch to GND. This combination makes the outputs flexible enough to connect them directly to many power supply shutdown pins or to external N-channel MOSFET switches.

The LTC2924 monitors the output voltage of each sequenced power supply via four input pins (IN1 to IN4). These inputs use precision comparators and a trimmed bandgap voltage reference to provide better than 1% accuracy. The power ON and power OFF voltage thresholds are set using resistive dividers for each of the four channels. The power ON threshold and the power OFF threshold are individually selectable on a channel by channel basis (see "Selecting the Hysteresis Current and IN Pin Feedback Resistors" in the data sheet for details).

The LTC2924 timer pin (TMR) is used to provide an optional delay between the completion of start-up of one supply and the start-up of the next power supply. The delay time is selected by placing a capacitor between the TMR pin and ground (delay = 200ms/µF), whereas floating the TMR pin removes any delay. The start-up delay can be different than the shutdown delay. Figure 3 shows a simple circuit where the shutdown delay is half the start-up delay.

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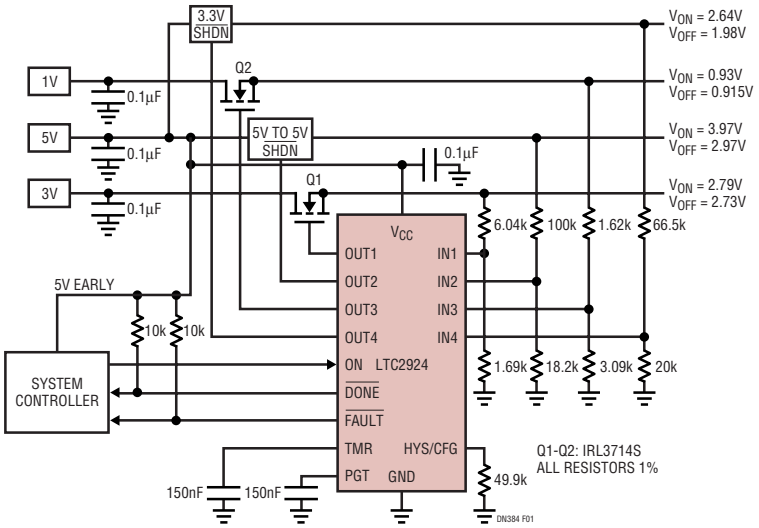

Figure 1. Typical Application with External N-Channel MOSFETs

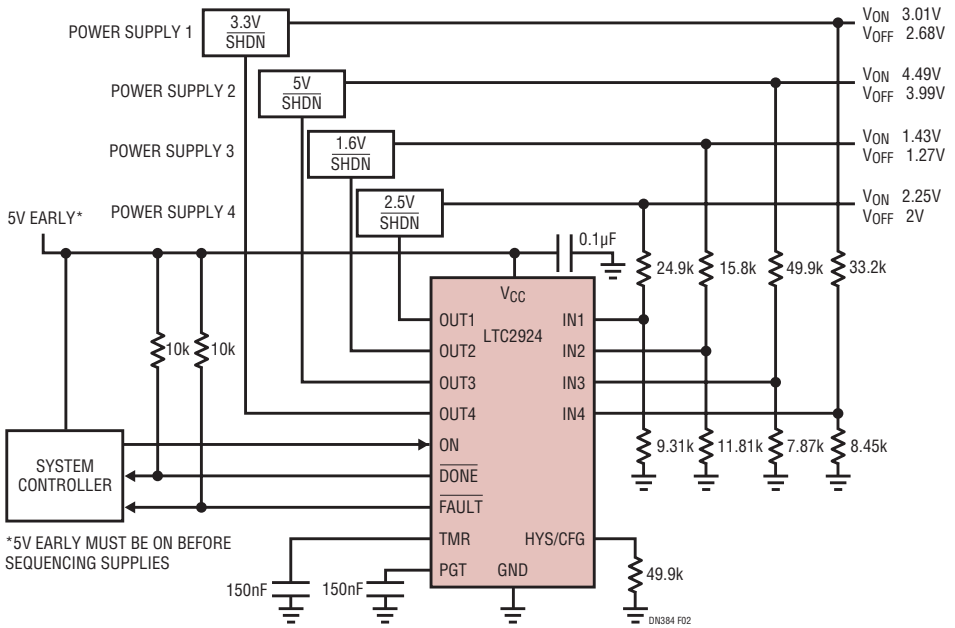

Figure 2. Four Power Supply Sequencer Using Shutdown Pins

The LTC2924 also includes a power good timer (PGT). The LTC2924 starts the PGT as each individual power supply is enabled. If any power supply fails to reach its nominal specified voltage within the allotted time interval, a power ON fault is detected.

Conclusion

The LTC2924 fits into a wide variety of power supply sequencing and monitoring applications. With very few external components and a 16-pin narrow SSOP, an LTC2924-based sequencing solution requires very little board space.

The power supply enable pins require no configuration by the designer, yet are versatile enough to directly drive shutdown pins or external N-channel MOSFETs. Soft-start of power supplies can be achieved simply by adding a capacitor. If the sequencing of more than four power supplies is required, the LTC2924 can be cascaded to sequence a virtually unlimited number of power supplies. Tailoring the LTC2924 to a specific application requires no software and designs can be fine tuned during system integration simply by changing resistor and capacitor values. Ease of design, low component cost, and a small footprint make the LTC2924 an excellent choice for power supply sequencing and monitoring.

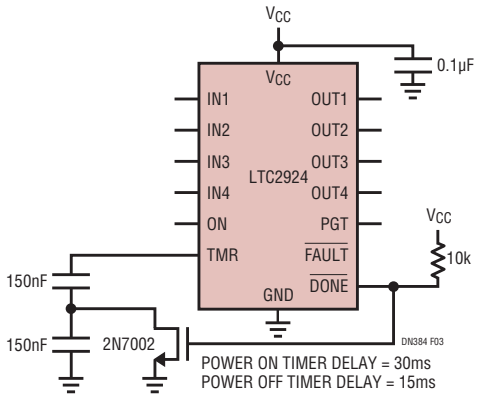

Figure 3. Programming Different ON/OFF Delays

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Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

dn384 LT/TP 0306 409K • PRINTED IN THE USA

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